TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		Attorney's Docket Number 70357
		U.S. Application No. (if known, see 37 C.F.R. 1.5) 10/019696
INTERNATIONAL APPLICATION NO. PCT/DE00/01396	INTERNATIONAL FILING DATE 4/May/2000	PRIORITY DATE CLAIMED 5/May/1999
TITLE OF INVENTION CHIP CARRIER FOR A CHIP MODULE AND METHOD OF MANUFACTURING THE CHIP MODULE		
APPLICANT(S) FOR DO/EO/US FINN et al.		

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a FIRST submission of items concerning a filing under 35 U.S.C. 371.

2. [] This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371

3. [X] This express request to begin national examination procedures (35 U.S.C. 371(f) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. [X] A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. [X] A copy of the International Application as filed (35 U.S.C. 371(C)(2))
   a. [ ] is transmitted herewith (required only If not transmitted by the International Bureau).
   b. [X] has been transmitted by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).

6. [X] A translation of the International Application into English (35 U.S.C. 371(c)(2)).

7. [ ] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are transmitted herewith (required only if not transmitted by the International Bureau).
   b. [ ] have been transmitted by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [ ] have not been made and will not be made.

8. [ ] A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).

9. [] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).

10. [ ] A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other documents (s) or information included:

11. [X] An Information Disclosure Statement under 37 CFR 1.97 and 1.98

12. [] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3 31 is included.

13. [X] A FIRST preliminary amendment.
    [ ] A SECOND or SUBSEQUENT preliminary amendment.

14. [X] A substitute specification.

15. [ ] A change of power of attorney and/or address letter.

16. [X] Other items or information:
    Formal Drawings (2 sheets)
    Copy of Express Mail Receipt No. EL 346 229 420 US
    Copies of Cited References (11)
    Marked Up Copy of the Translation

U.S. Appl. 10/019696	International Application No. PCT/DE00/01396	Attorney's Docket Number 70357

17. [X] The following fees are submitted:	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5)):		
Search Report has been prepared by the EPO or JPO $890.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) $710.00		
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) $740.00		
Neither international preliminary examination fee (37 CFR 1.482 nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO $1,040.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) $100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 890.00	
Surcharge of $130.00 for furnishing the oath or declaration later than [ ]20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(e))	$	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total Claims	14 - 20 =		X $ 18.00	$	
Independent claims	3 - 3 =		X $ 84.00	$	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $270.00	$	
TOTAL OF ABOVE CALCULATIONS =				$	

Reduction of 1/2 for filing small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1,28)	$ 445.00	
SUBTOTAL =	$ 445.00	
Processing fee of $130.00 for furnishing the English translation late than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +	$	
TOTAL NATIONAL FEE =	$ 445.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property +	$	
TOTAL FEES ENCLOSED =	$ 445.00	
	Amount to be: refunded	$
	charged	$

a. [X] A check in the amount of $ 445.00 to cover the above fees is enclosed.

b. [ ] Please charge my Deposit Account No. 13-0410 in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. [X] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 13 0410. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

Send all correspondence to:

McGLEW AND TUTTLE, P.C.
Scarborough Station
Scarborough, NY 10510-0827

Signature

John James McGlew
Name

31,903
Registration Number

The PTO did not receive the following listed item(s) No check

[redacted]

ATTORNEY DOCKET NO: 70357

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : FINN et al.
PCT No : PCT/DE00/01396
Filed : November 5, 2001
For : CHIP CARRIER FOR...
Dated : November 2, 2001

Hon. Commissioner of Patents
and Trademarks
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Prior to initial examination, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Please replace the specification originally filed, with the enclosed substitute specification. A marked up copy of the original specification is attached. Applicant states that no new matter has been added.

IN THE CLAIMS:

Please rewrite the claims as follows:

1. (AMENDED) A chip carrier for forming a chip module, the chip carrier comprising:

a substrate formed by a carrier film; and

connection leads arranged on the substrate, said connection leads comprising stripes and extend parallel over the substrate, said connection leads comprising electrically conductive

connection strands arranged on said substrate in a single plane and extending in a planar direction over the entire substrate surface and having a longitudinal expansion flush with the substrate surface.

2. (AMENDED) A chip carrier according to claim 1, wherein the carrier film is provided with at least one additional conductive counter-strand on a side opposite the connection strands to generate a capacitance, wherein the insulating carrier film is arranged as an intermediate layer between the connection strands on the one hand and the counter-strand on the other.

3. (AMENDED) A chip carrier according to claim 1, wherein said connection strands are at least sectionally provided with a connecting material coating for contacting with the contact metallizations of a chip.

4. (AMENDED) A chip carrier according to claim 1, wherein said connection strands are at least sectionally provided with a contact metallization for contacting with the contact metallizations of a chip.

5. (AMENDED) A chip carrier according to claim 1, wherein said connection strands are connected with the terminals of a coil unit.

6. (AMENDED) A chip module, comprising:

a chip carrier comprising a substrate formed by a carrier film and connection leads arranged on the substrate, said connection leads comprising stripes and extend parallel over the substrate, said connection leads comprising electrically conductive connection strands arranged on said substrate in a single plane and extending in a planar direction over the entire substrate surface and having a longitudinal expansion flush with the substrate surface; and

connecting surfaces with elevated contact metallizations, said contact metallizations being in contact with a top side of said connection strands facing away from the carrier film.

7. (AMENDED) A chip module according to claim 6, wherein the connection strands are in contact with the contact metallizations of the chip and are connected with the terminals of a coil unit.

8. (AMENDED) A method of manufacturing a chip module with a chip carrier comprising a substrate formed by a carrier film and connection leads arranged on the substrate, said connection leads comprising stripes and extend parallel over the substrate, said connection leads comprising electrically conductive connection strands arranged on said substrate in a single plane and extending in a planar direction over the entire substrate surface and having a longitudinal expansion flush with the substrate surface and connecting surfaces with elevated contact metallizations, said contact metallizations being in contact with a top side of said connection strands facing away from the carrier film, the method comprising the steps of:

applying at least two electrically conductive connection strands to one side of the carrier film so that connection strands lie parallel to each other in a single plane, and extend in a planar direction over the carrier film; and

contacting contact metallizations of the chip with the connection strands, so that a contact metallization of the chip is contacted with a respective connection strand.

9. (AMENDED) A method of manufacturing a chip module according to claim 8, wherein the connection strands are contacted with a coil unit before contacting the connection strands with the chip.

10. (AMENDED) A method of manufacturing a chip module according to claim 8, wherein the connection strands are continuously applied to the carrier film in such a way that the connection strands and carrier film are provided as continuous strands, and moved against each other continuously in a contact area while forming an adhesion.

11. (AMENDED) A method according to claim 10, wherein the carrier film is provided with window openings at defined distances before forming the contact area with the connection strands, so that the window openings in the subsequently formed contact area are covered by the connection strands while forming pocket-like contact receptacles.

12. (AMENDED) A method according to claim 8, wherein the carrier film is coated

with at least one additional electrically conductive counter-strand on a side opposite the side intended for applying the connection strands.

13. (AMENDED) A method according to claim 8, wherein the connection strands and/or the at least one counter strand are applied to the carrier film in a laminating process.

14. (AMENDED) A method according to claim 13, wherein the adhesion between the connection strands and/or at least one counter-strand and carrier film is generated via a hot melt application.

REMARKS

Claims 1 through 14 are in this application and are presented for consideration. Claims 1 through 14 have been amended. The amended claims present the same subject matter as the original claims but have been amended to adapt them to the U. S. style. The new claims present subject matter similar to the original claims, but in a different form.

The specification and claims have been amended in order to place this application in better form. The reference to claims in the specification has been deleted or amended. Appropriate headings have been added. No new matter has been added.

Favorable action on the merits is respectfully requested.

Respectfully submitted
for Applicant,

By: _____
John James McGlew
Registration No. 31,903
McGLEW AND TUTTLE, P.C.

JJM:jj
70357.1

Enclosed: Version of Claims Showing Changes, Substitute Specification and Marked up copy of Translation

DATED: November 2, 2001
SCARBOROUGH STATION
SCARBOROUGH, NEW YORK 10510-0827
(914) 941-5600

SHOULD ANY OTHER FEE BE REQUIRED, THE PATENT AND TRADEMARK OFFICE IS HEREBY REQUESTED TO CHARGE SUCH FEE TO OUR DEPOSIT ACCOUNT 13-0410.

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS EXPRESS MAIL IN AN ENVELOPE ADDRESSED TO: COMMISSIONER OF PATENTS AND TRADEMARKS, WASHINGTON, D.C. 20231, NO.: EL 346 229 420 US

McGLEW AND TUTTLE, P.C.
SCARBOROUGH STATION, SCARBOROUGH, NY 10510-0827

BY: _____ DATE: November 2, 2001

1;. (AMENDED) A chip carrier for forming a chip module ~~with~~, the chip carrier comprising:

a substrate formed by a carrier film; and

connection leads arranged on the substrate, ~~wherein the~~said connection leads ~~are designed like~~comprising stripes and extend parallel over the substrate, ~~characterized in that the~~said connection leads ~~consist of~~comprising electrically conductive connection strands ~~(12, 13) applied to the substrate, and the substrate is formed by a carrier film (11).~~

~~2. The~~ strands arranged on said substrate in a single plane and extending in a planar direction over the entire substrate surface and having a longitudinal expansion flush with the substrate surface.

2. (AMENDED) A chip carrier according to claim 1, ~~characterized in that~~wherein the carrier film ~~(11)~~ is provided with at least one additional conductive counter-strand ~~(27)~~ on ~~its~~a side opposite the connection strands ~~(12, 13)~~ to generate a ~~capacity~~capacitance, wherein the insulating carrier film is arranged as an intermediate layer between the connection strands on the one hand and the counter-strand on the other.

3. ~~The~~(AMENDED) A chip carrier according to claim 1 ~~or 2~~, ~~characterized by the fact that the~~wherein said connection strands ~~(12, 13)~~ are at least sectionally provided with a connecting material coating for contacting with the contact metallizations ~~(15, 16)~~ of a chip ~~(14)~~.

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4. ~~The~~(AMENDED) A chip carrier according to ~~one of the preceding~~ claims 1, ~~characterized in that the~~wherein said connection strands ~~(12, 13)~~ are at least sectionally provided ~~30~~ with a contact metallization for contacting with the contact metallizations ~~(15, 16)~~ of a chip ~~(14)~~.

5. ~~The~~(AMENDED) A chip carrier according to ~~one of the preceding~~ claims1, ~~characterized in that the~~wherien said connection strands ~~(12, 13)~~ are connected with the terminals of a coil unit.

~~6. The~~ 6. (AMENDED) A chip module, comprising:

a chip carrier comprising a substrate formed by a carrier film and connection leads arranged on the substrate, said connection leads comprising stripes and extend parallel over the substrate, said connection leads comprising electrically conductive connection strands arranged on said substrate in a single plane and extending in a planar direction over the entire substrate surface and having a longitudinal expansion flush with the substrate surface; and

connecting surfaces with elevated contact metallizations, said contact metallizations being in contact with a top side of said connection strands facing away from the carrier film.

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7. ~~The~~(AMENDED) A chip module according to claim 6, ~~characterized in that~~wherein

the connection strands ~~(12, 13)~~are in contacted with the contact metallizations ~~(15, 16)~~ of the chip ~~(14)~~and are connected with the terminals of ~~the~~a coil unit.
End Of Moved Text

8. (AMENDED) A method of manufacturing a chip module with a chip carrier ~~according to one of claims 1 to 5 and a chip having~~comprising a substrate formed by a carrier film and connection leads arranged on the substrate, said connection leads comprising stripes and extend parallel over the substrate, said connection leads comprising electrically conductive connection strands arranged on said substrate in a single plane and extending in a planar direction over the entire substrate surface and having a longitudinal expansion flush with the substrate surface and connecting surfaces with elevated contact metallizations, ~~characterized in that to the~~said contact metallizations ~~(15, 16) of the chip (14) are~~being in contacted with ~~the~~a top side ~~(21)~~ of ~~the~~said connection strands ~~(12, 13)~~.

Text Was Moved From Here. !

~~8. A method of manufacturing a chip module according to claim 6 or 7, characterized by the following steps:~~ facing away from the carrier film, the method comprising the steps of:

applying at least two electrically conductive connection strands ~~(12, 13)~~ to one side of the carrier film ~~(11)~~, so that ~~the~~ connection strands ~~extend parallel~~lie parallel to each other in a single plane, and extend in a planar direction over the carrier ~~surface,~~film; and ~~-~~

contacting contact metallizations ~~(15, 16)~~ of the chip ~~(14)~~ with the connection strands, so that a contact metallization of the chip is contacted with a respective connection strand.

9. ~~The~~(AMENDED) A method of manufacturing a chip module according to claim 8, ~~30 characterized in that, before contacting the connection strands (12, 13) with the chip (14),~~wherein the connection strands are contacted with ~~the coil unit.~~

~~10. The~~a coil unit before contacting the connection strands with the chip.

10. (AMENDED) A method of manufacturing a chip module according to claim 8 ~~or 9 characterized in that~~, wherein the connection strands ~~(12, 13)~~ are continuously applied to the carrier film ~~(11)~~, in such a way that the connection strands and carrier film are ~~prepared~~provided as continuous strands, and moved against each other continuously in a contact area ~~(38)~~ while forming an adhesion. ~~to~~

11. ~~The~~(AMENDED) A method according to claim 10, ~~characterized in that~~wherien the carrier film is provided with window openings at defined distances before forming the contact area ~~(38)~~ with the connection strands ~~(12, 13)~~, so that the window openings in the subsequently formed contact area are covered by the connection strands ~~(12, 13)~~ while forming pocket-like contact receptacles ~~(23, 24)~~.

12. ~~The~~ (AMENDED) A method according to ~~one of~~ claims 8 ~~to 11~~, ~~characterized in that~~wherein the carrier film ~~(11)~~ is coated with at least one additional electrically conductive

counter-strand ~~(27)~~ on ~~the~~a side opposite the side intended for applying the connection strands ~~(12, 13)~~.

13. ~~The~~ (AMENDED) A method according to ~~one of~~ claims 8 ~~to 12~~, ~~characterized in that~~wherein the connection strands ~~(12, 13)~~ and/or the at least one counter strand ~~(27)~~ are applied to the carrier film ~~(11)~~ in a laminating process.

14. ~~The~~ (AMENDED) A method according to claim 13, ~~characterized in that~~wherein the adhesion between the connection strands ~~(12, 13)~~ and/or at least one counter-strand ~~(27)~~ and carrier film ~~(11)~~ is generated via a hot_melt application.

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(71)(72) Anmelder und Erfinder: FINN, David [IE/DE]; Steigmühlenweg 16a, D–87629 Füssen–Weissensee (DE). RIETZLER, Manfred [DE/DE]; Am Alsterberg 10, D–87616 Marktoberdorf (DE).

(74) Anwalt: TAPPE, Hartmut; Böck + Tappe Kollegen, Kantstrasse 40, D–97074 Würzburg (DE).

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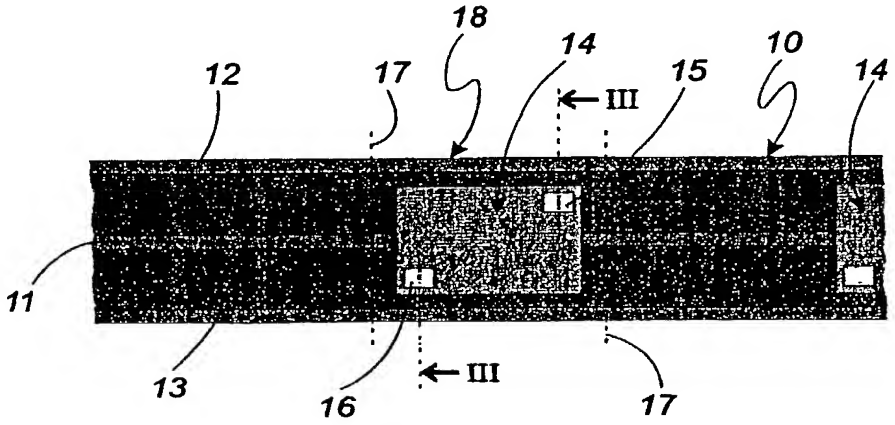
Veröffentlicht
Mit internationalem Recherchenbericht.
Vor Ablauf der für Änderungen der Ansprüche zugelassenen Frist; Veröffentlichung wird wiederholt falls Änderungen eintreffen.

(54) Title: CHIP HOLDER FOR A CHIP MODULE AND METHOD FOR PRODUCING SAID CHIP MODULE

(54) Bezeichnung: CHIPTRÄGER FUR EIN CHIPMODUL UND VERFAHREN ZUR HERSTELLUNG DES CHIPMODULS

(57) Abstract

The invention relates to a chip holder for forming a chip module (18) comprising a substrate and supply leads placed on the substrate, wherein the supply leads are shaped in the form of strips and extend in a parallel manner along the substrate and wherein the supply leads consist of electrically conductive connecting strips (12, 13) mounted on the substrate and the substrate is formed by a carrier foil (11).



(57) Zusammenfassung

Die Erfindung betrifft einen Chipträger zur Ausbildung eines Chipmoduls (18) mit einem Substrat und auf dem Substrat angeordneten Anschlußleitern, wobei die Anschlußleiter streifenförmig ausgebildet sind und sich parallel über das Substrat erstrecken und wobei die Anschlußleiter aus auf das Substrat aufgebrachten elektrisch leitfähigen Anschlußbändern (12, 13) bestehen und das Substrat durch eine Trägerfolie (11) gebildet ist.

ENGLISH TRANSLATION 2/prts

CHIP CARRIER FOR A C141P MODULE AND METHOD OF MANUFACTURING THE CHIP MODULE.

The present invention relates to a chip carrier with a substrate and connection leads arranged on the substrate, wherein the connection leads are designed like stripes and extend parallel over the substrate. In addition, the invention relates to a chip module manufactured using the chip carrier, and a method of manufacturing such a chip module.

Chip modules are usually manufactured using chip carriers whose surface is provided with a printed circuit structure for connection with elevated contact metallizations of the chip. The use of printed circuit structures manufactured in etching processes does enable any printed circuit structures desired, in particular those with a complex design. However, just the provision or manufacture of the conventional chip carriers independently of the actual contacting process with the chip for manufacturing the chip module already requires a complex and correspondingly expensive procedure. The use of etching techniques requires an appropriate structure for the carrier layer of the substrate, which in addition to a so-called etch-stop layer must also be provided

with a lacquer coating when using lithographic processes for defining the printed circuit structure.

Known from DE 195 41 039 A1 is a chip module with a chip carrier, in which the connection leads formed on an insulation layer extend in a stripe-like design and mutually parallel over the insulation layer of the substrate, and are each allocated to an elevated contact metallization of a chip. To manufacture the known chip module, the individual substrates of the chip carriers are arranged on a continuous substrate carrier, which is connected with the individual substrates via the connection leads extending continuously over the substrate carrier. In the known method, the film-like substrate carrier is used only to connect the connection leads with the substrate.

Proceeding from known prior art, the object of the invention is to provide a chip carrier for a chip module or a method of manufacturing a chip module, which exhibits a particularly simple design relative to the known chip modules, and hence opens the door to particularly cost-effective manufacture.

This object is achieved using a chip carrier with the features set forth in claim 1.

In the chip carrier according to the invention, the connection leads consist of electrically conductive connection strands placed on the substrate, and the substrate is formed by a carrier film. i

Designing the connection leads as connection strands that are completely independent of the carrier film makes it possible not to have to manufacture the connection leads based on an expensive etching technique. Therefore, the chip carrier according to the invention consists I of a combination of a carrier film and connection strands, which each represent independent elements in the initial state, so that no special technologies, e.g., the use of an etching process, are required for manufacturing the chip carrier, but rather a simple connecting or joining process, wherein the substrate is directly formed by the carrier film. Having the substrate serve as the carrier film also enables substrates with a particularly flat design.

In a particularly preferred embodiment of the chip carrier, the side of the carrier film opposite the connection strands is provided with at least one additional conductive strand, in which the insulating carrier film is arranged between the connection strands on the one hand and the additional conductive strand on the other, forming an intermediate layer.

Adding this at least one conductive strand on the opposite side of the carrier film yields a capacitor structure that is arranged in a parallel

circuit with the chip after the connection strands have been contacted with a chip. Precisely in the area of transponder technology, this special configuration of the chip module gives rise to the special advantage when contacting the connection strands with a coil unit that the range of the transponder unit formed by combining the chip and coil unit can be distinctly increased.

In particular with respect to the automated manufacture of chip modules using the chip carriers, it proves advantageous to provide the connection strands at least sectionally with a connecting material coating for contacting with the contact metallizations of the chip, so that the chip can be contacted directly on the connecting strands after providing the substrate without any additional intermediate step. This connecting material coating can consist of a connecting solder coating, or a coating of electrically conductive adhesive or the like.

Providing the connection strands at least sectionally with a contact metallization for contacting with the elevated contact metallizations of the chip makes it possible to obtain especially high-quality, i.e., reliable, connections, in particular due to the surface quality of the connection strands as unproved by the contact metallization. Otherwise, of course, connecting strands made out of copper or a copper alloy can be used to produce a direct connection with the contact metallizations of the chip, in particular if the contact metallizations of the chip exhibit a lead/tin alloy or similar alloys with a correspondingly low melting point.

If the connection strands of the chip carrier are connected with the terminals of the coil unit, the chip carrier can serve as the basic unit for manufacturing a transponder, wherein the basic unit need only be enhanced by contact with a chip.

Based on the chip module described above, it is also possible, as already mentioned above, to provide a transponder module in which the connection strands contacted with the contact metallizations of the chip are connected according to the invention with terminals of a coil unit.

In the chip module according to the invention, the contact metallizations of the chip are contacted with the top side of the connection strands of the chip carrier. In addition to the fact that the chip module can be manufactured with a simple flip-chip contact, this chip module structure offers the advantage of making the side of the substrate lying opposite the connection strands available for further applications.

If the connection strands contacted with the contact metallizations of the chip are additionally connected with the terminals of a coil unit, a transponder module with an especially simple structure is obtained.

The method according to the invention for manufacturing a chip module involves the following steps:

- applying at least two electrically conductive connection strands to one side of a carrier film, so that the connection strands extend

parallel over the carrier film, and

- contacting contact metallizations of the chip with the connection strands, so that a contact metallization of the chip is contacted with a respective connection strand.

As already emphasized at the outset while describing the structure of the - chip module according to the invention, the manufacturing process is characterized by the lowest possible number of steps, due to the fact that the substrate provided with connection leads is realized via a simple combination of connection strands with a carrier film, and the type of contacting according to the invention enables a simple flip-chip contacting.

If the connection strands are contacted with the coil unit before being contacted with the chip, a first portion of the manufacturing process, which can also be executed independently of the subsequent contacting with the chip, yields an intermediate product in the form of a chip carrier, which can be directly used for manufacturing transponder units.

One particularly economic variant of the method according to the invention can be implemented if the connection strands are continuously applied to the carrier film, so that the connection strands and the carrier film are provided as continuous strands, and moved continuously toward each other in a contacting area with the generation of an adhesion.

If the carrier film is provided with window openings at defined distances before forming the

contact area with the connection strands, so that the window openings in the subsequently formed contact area are covered by the connection strands while forming pocket-like contact receptacles, it becomes possible to manufacture a chip module even without the influence of a continuous process, in which the contact metallizations of the chip are contacted with the bottom side of the connection strands, and the chip itself is located on the side of the carrier film opposite the connection strands.

Therefore, this method variant enables the manufacture of an especially i flat or thin chip module.

A chip module with a capacitor structure can be manufactured in another method variant by placing at least one additional electrically conductive counter-strand on the side lying opposite the side intended for applying
the connection strands. This process can take place before or after
applying the connection strands on the carrier film.

One particularly easy and hence cost-effective way of implementing the method is made possible by applying the connection strands and/or at
to least one counter-strand on the carrier film in a lamination process.

In this connection, it is also advantageous to use a hot-melt coating to form an adhesion between the connection strands and/or the at least one counter-strand and the carrier film.

An embodiment of the chip module and a variant of the method of manufacturing the chip module shall be explained in greater detail below based on the drawings. Shown in:

Fig. 1 is a chip carrier for manufacturing a chip module, top view,

Fig. 2 is the chip carrier shown in Fig. I with a chip contacted thereupon to form a chip module;

Fig. 3 is a first embodiment of a chip module, sectional view;

Fig. 4 is a second embodiment of the chip module, sectional view;

Fig. 5 is a third embodiment of a chip module, sectional view;

Fig. 6 is an electrical equivalent circuit diagram for the substrate of the chip module shown in Fig. 5;

Fig. 7 is a diagrammatic view of a device for performing a variant of the method of manufacturing the chip module.

Fig. 1 shows a top view of a section of a chip carrier strand 10 with a carrier film 11 and connection strands 12 and 13 applied to one side of the carrier film 1 1-

Fig. 2 shows the chip carrier strand 10 depicted in Fig. 1 with numerous spaced chips 14 contacted on the chip carrier strand 10. As evident from Fig. 2, the chips 14 with their contact metallizations, also referred to as "bumps" in technical parlance, are contacted with connection strands 12, 13 in flip-chip technology in such a way that one bump 15 or 16 is allocated to a connection strand 12, 13 in an electrically conductive manner.

As indicated by separating lines 17 in Fig. 2, chip modules 18 are detached from the composite chip module held together by the chip carrier strand 10 via separating cuts through the chip carrier strand 10 after the chips 14 have contacted the chip carrier strand 10.

Fig. 3 shows a sectional view according to intersecting line III-III in Fig. 2. As evident, chip 14 is contacted in flip-chip technology with its bumps 15, 16 on the connection strands 12, 13 of the chip carrier 19 separated

out of the chip carrier strand 10 along separating lines 17. In this case, the carrier film 1 I forming the substrate of the chip carrier 19 consists of kapton, whose top side is covered with the connection strands 12, 13 made out of so-called E copper. To improve the surface quality of the connection strands 12. 13, the latter are coated with a contact

metallization in this case. Other electrically non-conductive materials can also be used for the chip carrier 19 or chip carrier strand 10, e.g., epoxy glass, polyester, polycarbonate and polyimide, wherein a flexible design of the carrier film 11, e.g., using polyimide, is advantageous, in particular when using a manufacturing process of the kind explained in greater detail below with reference to Fig. 7.

Fig. 4 shows a variant of a chip module 20 in which the chip 14 is contacted with a bottom side 22 of the connection strands 12, 13, as opposed to the chip module 18 shown in Fig. 3, where the chip 14 is contacted with a top side 21 of the connection strands 12, 13.

to To this end, pocket-like contact receptacles 23, 24 are formed in the areas of the carrier film of a chip carrier 28 covered by the connection strands 12, 13, and used to accommodate the bumps 15, 16 of the chip 14, Given the appropriate preparation of the surfaces of connection strands 12,

13, e.g., via contact metallization, the bumps 15, 16 can be directly

is contacted with the connection strands 12, 13, or a contacting process as shown in Fig. 4 can be performed, in which a separate bonding material, e.g., soldering material 25 situated between the bottom sides 22 of the connection strands 12, 13 and the bumps 15, 16 of the chip 14 is additionally provided.

Fig. 5 shows another embodiment of a chip module 26, in which, as opposed to the chip module 18 shown in Fig. 3, a counter-strand 27 is provided on the side of the carrier film I1 opposite the connection strands 12, 13, which is applied to the carrier film 1 1 in the same manner as the connection strands 12,13, and can consist of the same material as the connection strands 12, 13. The structure shown in Fig. 5 of opposing connection strands 12, 13 separated from each other by an insulating intermediate layer in the form

of the carrier layer I l on the one hand and the counter strand 27 on the other yields am electric capacitor arrangement whose circuit diagram is shown in fig. 6. According to Fig. 6, the structure of the substrate 28 yields an electrical serial connection of two capacitors arranged parallel to the chip 14.

Fig. 7 shows a possible variant for manufacturing a chip module, wherein

the system design shown in Fig. 7 enables in particular the manufacture of the chip module 20 shown in Fig. 4 in a continuous and interconnected arrangement. To this end, the system diagrammatically shown in Fig. 7 encompasses a supply roll 30 with carrier film 11 wound onto it, which is unrolled in the direction of arrow 31, and wound up at the end of the

system on a product roll 32. Located in the area between the supply roll 30 and product roll 32 are two supply rolls 33 and 34 with wound up connection strand 12 or 13. Located between the supply rolls 33 and 34 on the one hand and the product roll 32 on the other is a laminating roller 35. To manufacture a continuous, band-shaped and interconnected arrangement of chip carriers 28 or chip modules 20, as shown in fig. 4, the carrier film 11 is clocked and advanced in the direction of the arrow 31 according to Fig. 7, wherein window openings arc incorporated into the carrier film I l at the prescribed clock rate at defined intervals via a stamping device 36 to form the contact receptacles 23, 24 shown in Fig. 4. Downstream of the stamping device 36, the connection strands 12, 13 are supplied to the carrier film 11 from the supply rolls 33, 34, and then connected with the carrier film 1 I in a roll slit formed by the laminating roll 35 and a counter-roll 37 in a contact area 38. As a result of this joining or connecting process, the chip carrier 28 shown in cross section in Fig- 4 is therefore generated in continuous form downstream of the laminating roll 35, and wound on the product roll 32. The product roll 32 can now be used as a supply roll for a subsequent manufacturing process for the continuous or clocked contacting of chips 14 with the connection strands 12, 13, thus making it possible to manufacture continuously interconnected chip modules 20 as shown in Fig. 4.

To prepare for a subsequent manufacture of transponder units, coil units can also be contacted

with the connection strands after the laminating process. The coils can here be designed as desired. The coils can be arranged on a separate carrier, or have no carrier in a particularly advantageous variant, being applied directly to the carrier film and contacted with the connection strands. In this connection, the use of wire coils proves advantageous.

CLAIMS

1, A chip carrier for forming a chip module with a substrate and connection leads arranged on the substrate, wherein the connection leads are designed like stripes and extend parallel over the substrate,
characterized in that
the connection leads consist of electrically conductive connection strands (12, 13) applied to the substrate, and the substrate is formed by a carrier film (11).

2. The chip carrier according to claim 1,
characterized in that
the carrier film (11) is provided with at least one additional conductive counter-strand (27) on its side opposite the connection strands (12, 13) to generate a capacity, wherein the insulating carrier film is arranged as an intermediate layer between the connection strands on the one hand and the counter-strand on the

other.

3. The chip carrier according to claim 1 or 2,
characterized by the fact that
the connection strands (12, 13) are at least sectionally provided
with a connecting material coating for contacting with the contact
metallizations (15, 16) of a chip (14).

4. The chip carrier according to one of the preceding claims, characterized in that the connection strands (12, 13) are at least sectionally provided 30 with a contact metallization for contacting with the contact metallizations (15, 16) of a chip (14)

5. The chip carrier according to one of the preceding claims,
characterized in that
the connection strands (12, 13) are connected with the terminals of
a coil unit.

6. The chip module with a chip carrier according to one of claims 1 to
5 and a chip having connecting surfaces with elevated contact
metallizations,
characterized in that
to the contact metallizations (15, 16) of the chip (14) are contacted

with the top side (21) of the connection strands (12, 13).

7. The chip module according to claim 6,
characterized in that
the connection strands (12, 13) contacted with the contact metallizations (15, 16) of the chip (14) are connected with the terminals of the coil unit.

8. A method of manufacturing a chip module according to claim 6 or 7,
characterized by the following steps:
- applying at least two electrically conductive connection strands (12, 13) to one side of the carrier film (II), so that the connection strands extend parallel over the carrier surface, and
- contacting contact metallizations (15, 16) of the chip (14) with the connection strands, so that a contact metallization of the chip is contacted with a respective connection strand.

9. The method of manufacturing a chip module according to claim 8, 30 characterized in that, before contacting the connection strands (12, 13) with the chip (14), the connection strands are contacted with the coil unit.

10. The method of manufacturing a chip module according to claim 8 or 9,
characterized in that
the connection strands (12, 13) are continuously applied to the carrier film (11), in such a way that the connection strands and carrier film are prepared as continuous strands, and moved against each other continuously in a contact area (38) while forming an adhesion.

11. The method according to claim 10, characterized in that the carrier film is provided with window openings at defined distances before forming the contact area (38) with the connection strands (12, 13), so that the window openings in the subsequently
formed contact area are covered by the connection strands (12, 13)
while forming pocket-like contact receptacles (23, 24).

12. The method according to one of claims 8 to 1 1,
characterized in that
the carrier film (11) is coated with at least one additional
electrically conductive counter-strand (27) on the side opposite the
side intended for applying the connection strands (12, 13).

13. The method according to one of claims 8 to 12,
characterized in that
the connection strands (12, 13) and/or the at least one counter
strand (27) are applied to the carrier film (11) in a laminating

process.

14. The method according to claim 13, characterized in that the adhesion between the connection strands (12, 13) and/or at least 5 one counter-strand (27) and carrier film (11) is generated via a hotmelt application.

ABSTRACT

The invention relates to a chip carrier for manufacturing a chip module (18), with a substrate and connection leads arranged on the substrate,

wherein the connection leads are designed like stripes and extend parallel over the substrate, and wherein the connection leads consist of electrically conductive connection strands (12, 13) placed on the substrate, and the substrate is formed by a carrier film (11).

Docket # 70357

CHIP CARRIER FOR A CHIP MODULE AND METHOD OF MANUFACTURING THE CHIP MODULE

FIELD OF THE INVENTION

The present invention relates to a chip carrier with a substrate and connection leads arranged on the substrate, wherein the connection leads are designed like stripes and extend parallel over the substrate. In addition, the invention relates to a chip module manufactured using the chip carrier, and a method of manufacturing such a chip module.

BACKGROUND OF THE INVENTION

Chip modules are usually manufactured using chip carriers whose surface is provided

with a printed circuit structure for connection with elevated contact metallizations of the chip. The use of printed circuit structures manufactured in etching processes does enable any printed circuit structures desired, in particular those with a complex design. However, just the provision or manufacture of the conventional chip carriers independently of the actual contacting process with the chip for manufacturing the chip module already requires a complex and correspondingly expensive procedure. The use of etching techniques requires an appropriate structure for the carrier layer of the substrate, which in addition to a so-called etch-stop layer must also be provided with a lacquer coating when using lithographic processes for defining the printed circuit structure.

Known from DE 195 41 039 A1 is a chip module with a chip carrier, in which the connection leads formed on an insulation layer extend in a stripe-like design and mutually parallel over the insulation layer of the substrate, and are each allocated to an elevated contact metallization of a chip. To manufacture the known chip module, the individual substrates of the chip carriers are arranged on a continuous substrate carrier, which is connected with the individual substrates via the connection leads extending continuously over the substrate carrier. In the known method, the film-like substrate carrier is used only to connect the connection leads with the substrate.

Known from DE 196 01 203 A1 are a data carrier card and a method of its manufacture, in which the data carrier card consists of a flat, injectionmolded plastic card body with at least one recess, on which three dimensionally guided printed conductors are applied. A chip can be electrically connected with the printed conductors in the recess, and then have a protective layer

cast around it to form the data carrier card.

EP 0 421 343 A2 describes a chip carrier for the connection and electromagnetic shielding of a single chip. The chip carrier has a complex, curved structure with discontinuous connection leads formed on the surface of the chip carrier.

EP 0 682 321 A2 shows a chip carrier to be arranged in a card body. The chip carrier exhibits a carrier substrate with connection leads discontinuously formed on the surface.

EP 0 391 790 Al describes a chip module or a method of manufacturing an encapsulated chip module with a chip, in which a structured metal film is applied to a carrier film to form connection leads.

FR 2 756 955 A1 describes a method of contacting a chip with a coil on a card-shaped carrier material, which is provided with a printed board arrangement in the form of a coil.

SUMMARY AND OBJECTS OF THE INVENTION

Proceeding from known prior art, the object of the invention is to provide a chip carrier for a chip module or a method of manufacturing a chip module, which exhibits a particularly simple design relative to the known chip modules, and hence opens the door to particularly cost-effective manufacture.

This object is achieved using a chip carrier with for forming a chip module with a substrate and connection leads arranged on the substrate. The connection leads are designed like stripes and extend parallel over the substrate. In the chip carrier according to the invention, the connection leads consist of electrically conductive connection strands placed on the

substrate, and the substrate is formed by a carrier film.

Designing the connection leads as connection strands that are completely independent of the carrier film makes it possible not to have to manufacture the connection leads based on an expensive etching technique. Therefore, the chip carrier according to the invention consists of a combination of a carrier film and connection strands, which each represent independent elements in the initial state, so that no special technologies, e.g., the use of an etching process, are required for manufacturing the chip carrier, but rather a simple connecting or joining process, wherein the substrate is directly formed by the carrier film. Having the substrate serve as the carrier film also enables substrates with a particularly flat design.

In a particularly preferred embodiment of the chip carrier, the side of the carrier film opposite the connection strands is provided with at least one additional conductive strand, in which the insulating carrier film is arranged between the connection strands on the one hand and the additional conductive strand on the other, forming an intermediate layer.

Adding this at least one conductive strand on the opposite side of the carrier film yields a capacitor structure that is arranged in a parallel circuit with the chip after the connection strands have been contacted with a chip. Precisely in the area of transponder technology, this special configuration of the chip module gives rise to the special advantage when contacting the connection strands with a coil unit that the range of the transponder unit formed by combining the chip and coil unit can be distinctly increased.

In particular with respect to the automated manufacture of chip modules using the chip carriers, it proves advantageous to provide the connection strands at least sectionally with a

connecting material coating for contacting with the contact metallizations of the chip, so that the chip can be contacted directly on the connecting strands after providing the substrate without any additional intermediate step. This connecting material coating can consist of a connecting solder coating, or a coating of electrically conductive adhesive or the like.

Providing the connection strands at least sectionally with a contact metallization for contacting with the elevated contact metallizations of the chip makes it possible to obtain especially high-quality, i.e., reliable, connections, in particular due to the surface quality of the connection strands as unproved by the contact metallization. Otherwise, of course, connecting strands made out of copper or a copper alloy can be used to produce a direct connection with the contact metallizations of the chip, in particular if the contact metallizations of the chip exhibit a lead/tin alloy or similar alloys with a correspondingly low melting point.

If the connection strands of the chip carrier arc connected with the terminals of the coil unit, the chip carrier can serve as the basic unit for manufacturing a transponder, wherein the basic unit need only be enhanced by contact with a chip.

Based on the chip module described above, it is also possible, as already mentioned above, to provide a transponder module in which the connection strands contacted with the contact metallizations of the chip are connected according to the invention with terminals of a coil unit.

In the chip module according to the invention, the contact metallizations of the chip are contacted with the top side of the connection strands of the chip carrier. In addition to the fact that the chip module can be manufactured with a simple flip-chip contact, this chip module

structure offers the advantage of making the side of the substrate lying opposite the connection strands available for further applications.

If the connection strands contacted with the contact metallizations of the chip are additionally connected with the terminals of a coil unit, a transponder module with an especially simple structure is obtained.

The method according to the invention of manufacturing a chip module involves the following steps:

- applying at least two electrically conductive connection strands to one side of the carrier film, so that the connection strands lie parallel to each other in a single plane, and extend in a planar direction over the carrier film, and

- contacting contact metallizations of the chip with the connection strands, so that a contact metallization of the chip is contacted with a respective connection strand.

As already emphasized at the outset while describing the structure of the chip module according to the invention, the manufacturing process is characterized by the lowest possible number of steps, due to the fact that the substrate provided with connection leads is realized via a simple combination of connection strands with a carrier film, arid the type of contacting according to the invention enables a simple flip-chip contacting.

If the connection strands are contacted with the coil unit before being contacted with the chip, a first portion of the manufacturing process, which can also be executed independently of the subsequent contacting with the chip, yields an intermediate product in the form of a chip carrier, which can be directly used for manufacturing transponder units.

One particularly economic variant of the method according to the invention can be implemented if the connection strands are continuously applied to the carrier filet, so that the connection strands and the carrier film are provided as continuous strands, and moved continuously toward each other in a contact area with the generation of an adhesion.

If the carrier film is provided with window openings at defined distances before forming the contact area with the connection strands, so that the window openings in the subsequently formed contact area are covered by the connection strands while forming pocket-like contact receptacles, it becomes possible to manufacture a chip module even without the influence of a continuous process, in which the contact metallizations of the chip are contacted with the bottom side of the connection strands, and the chip itself is located on the side of the carrier film opposite the connection strands.

Therefore, this method variant enables the manufacture of an especially i flat or thin chip module.

A chip module with a capacitor structure can be manufactured in another method variant by placing at least one additional electrically conductive counter-strand on the side lying opposite the side intended for applying the connection strands. This process can take place before or after applying the connection strands on the carrier film.

One particularly easy and hence cost-effective way of implementing the method is made possible by applying the connection strands and/or at least one counter-strand on the carrier film in a lamination process. In this connection, it is also advantageous to use a hot-melt coating to form an adhesion between the connection strands and/or the at least one counter-strand and

the carrier film.

An embodiment of the chip module and a variant of the method of manufacturing the chip module shall be explained in greater detail below based on the drawings.

The various features of novelty which characterize the invention are pointed out with particularity in the claims annexed to and forming a part of this disclosure. For a better understanding of the invention, its operating advantages and specific objects attained by its uses, reference is made to the accompanying drawings and descriptive matter in which preferred embodiments of the invention are illustrated.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

Fig. 1 is a top view of a chip carrier for manufacturing a chip module;

Fig. 2 is a view of the chip carrier shown in Fig. 1 with a chip in contact thereupon to form a chip module;

Fig. 3 is a sectional view of a first embodiment of a chip module;

Fig. 4 is a sectional view of a second embodiment of the chip module;

Fig. 5 is a sectional view of a third embodiment of a chip module;

Fig. 6 is a sectional view of an electrical equivalent circuit diagram for the substrate of the chip module shown in Fig. 5; and

Fig. 7 is a diagrammatic view of a device for performing a variant of the method of

manufacturing the chip module.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to the drawings in particular, Fig. 1 shows a top view of a section of a chip carrier strand 10 with a carrier film 11 and connection strands 12 and 13 applied to one side of the carrier film 11.

Fig. 2 shows the chip carrier strand 10 depicted in Fig. 1 with numerous spaced chips 14 contacted on the chip carrier strand 10. As evident from Fig. 2, the chips 14 with their contact metallizations, also referred to as "bumps" in technical parlance, are placed in contact with connection strands 12, 13 in flip-chip technology in such a way that one bump 15 or 16 is allocated to a connection strand 12, 13 in an electrically conductive manner.

As indicated by separating lines 17 in Fig. 2, chip modules 18 are detached from the composite chip module held together by the chip carrier strand 10 via separating cuts through the chip carrier strand 10 after the chips 14 have contacted the chip carrier strand 10.

Fig. 3 shows a sectional view according to intersecting line III-III in Fig. 2. As evident, chip 14 is in contact in flip-chip technology with its bumps 15, 16 on the connection strands 12, 13 of the chip carrier 19 separated out of the chip carrier strand 10 along separating lines 17. In this case, the carrier film 11 forming the substrate of the chip carrier 19 consists of kapton, whose top side is covered with the connection strands 12, 13 made out of so-called E copper. To improve the surface quality of the connection strands 12. 13, the latter are coated with a contact metallization in this case. Other electrically non-conductive materials can also be used

for the chip carrier 19 or chip carrier strand 10, e.g., epoxy glass, polyester, polycarbonate and polyimide, wherein a flexible design of the carrier film 11, e.g., using polyimide, is advantageous, in particular when using a manufacturing process of the kind explained in greater detail below with reference to Fig. 7.

Fig. 4 shows a variant of a chip module 20 in which the chip 14 is placed in contact with a bottom side 22 of the connection strands 12, 13, as opposed to the chip module 18 shown in Fig. 3, where the chip 14 is in contact with a top side 21 of the connection strands 12, 13.

To this end, pocket-like contact receptacles 23, 24 are formed in the areas of the carrier film 11 of a chip carrier 28 covered by the connection strands 12, 13, and used to accommodate the bumps 15, 16 of the chip 14. Given the appropriate preparation of the surfaces of connection strands 12, 13, e.g., via contact metallization, the bumps 15, 16 can be directly in contact with the connection strands 12, 13, or a contacting process as shown in Fig. 4 can be performed, in which a separate bonding material, e.g., soldering material 25 situated between the bottom sides 22 of the connection strands 12, 13 and the bumps 15, 16 of the chip 14 is additionally provided.

Fig. 5 shows another embodiment of a chip module 26, in which, as opposed to the chip module 18 shown in Fig. 3, a counter-strand 27 is provided on the side of the carrier film 11 opposite the connection strands 12, 13, which is applied to the carrier film 11 in the same manner as the connection strands 12,13, and can consist of the same material as the connection strands 12, 13.

The structure shown in Fig. 5 of opposing connection strands 12, 13 separated from

each other by an insulating intermediate layer in the form of the carrier layer 11 on the one hand and the counter strand 27 on the other yields an electric capacitor arrangement whose circuit diagram is shown in Fig. 6. According to Fig. 6, the structure of the substrate 28 yields an electrical serial connection of two capacitors arranged parallel to the chip 14.

Fig. 7 shows a possible variant for manufacturing a chip module, wherein the system design shown in Fig. 7 enables in particular the manufacture of the chip module 20 shown in Fig. 4 in a continuous and interconnected arrangement. To this end, the system diagrammatically shown in Fig. 7 encompasses a supply roll 30 with carrier film 11 wound onto it, which is unrolled in the direction of arrow 31, and wound up at the end of the system on a product roll 32. Located in the area between the supply roll 30 and product roll 32 are two supply rolls 33 and 34 with wound up connection strand 12 or 13. Located between the supply rolls 33 and 34 on the one hand and the product roll 32 on the other is a laminating roller 35. To manufacture a continuous, band-shaped and interconnected arrangement of chip carriers 28 or chip modules 20, as shown in Fig. 4,

the carrier film 11 is clocked and advanced in the direction of the arrow 31 according to Fig. 7, wherein window openings are incorporated into the carrier film 11 at the prescribed clock rate at defined intervals via a stamping device 36 to form the contact receptacles 23, 24 shown in Fig. 4. Downstream of the stamping device 36, the connection strands 12, 13

are supplied to the carrier film 11 from the supply rolls 33, 34, and then connected with the carrier film 11 in a roll slit formed by the laminating roll 35 and a counter-roll 37 in a contact area 38. As a result of this joining or connecting process, the chip carrier 28 shown in cross

section in Fig. 4 is therefore generated in continuous form downstream of the laminating roll 35, and wound on the product roll 32. The product roll 32 can now be used as a supply roll for a subsequent manufacturing process for the continuous or clocked contacting of chips 14 with the connection strands 12, 13, thus making it possible to manufacture continuously interconnected chip modules 20 as shown in Fig. 4.

To prepare for a subsequent manufacture of transponder units, coil units can also be contacted with the connection strands after the laminating process. The coils can here be designed as desired. The coils can be arranged on a separate carrier, or have no carrier in a particularly advantageous variant, being applied directly to the carrier film and contacted with the connection strands. In this connection, the use of wire coils proves advantageous.

While specific embodiments of the invention have been shown and described in detail to illustrate the application of the principles of the invention, it will be understood that the invention may be embodied otherwise without departing from such principles.

ABSTRACT OF THE DISCLOSURE

A chip carrier for manufacturing a chip module (18), with a substrate and connection leads arranged on the substrate has connection leads designed like stripes and extending parallel over the substrate. The connection leads are electrically conductive connection strands (12, 13) placed on the substrate. The substrate is formed by a carrier film (11).

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Docket # 70357

CHIP CARRIER FOR A ~~C141P~~CHIP MODULE AND METHOD OF MANUFACTURING THE CHIP MODULE

FIELD OF THE INVENTION

The present invention relates to a chip carrier with a substrate and connection leads arranged on the substrate, wherein the connection leads are designed like stripes and extend parallel over the substrate. In addition, the invention relates to a chip module manufactured using the chip carrier, and a method of manufacturing such a chip module.

BACKGROUND OF THE INVENTION

Chip modules are usually manufactured using chip carriers whose surface is provided with a printed circuit structure for connection with elevated contact metallizations of the chip.

The use of printed circuit structures manufactured in etching processes does enable any printed circuit structures desired, in particular those with a complex design. However, just the provision or manufacture of the conventional chip carriers independently of the actual contacting process with the chip for manufacturing the chip module already requires a complex and correspondingly expensive procedure. The use of etching techniques requires an appropriate structure for the carrier layer of the substrate, which in addition to a so-called etch-stop layer must also be provided with a lacquer coating when using lithographic processes for defining the printed circuit structure.

Known from DE 195 41 039 A1 is a chip module with a chip carrier, in which the connection leads formed on an insulation layer extend in a stripe-like design and mutually parallel over the insulation layer of the substrate, and are each allocated to an elevated contact metallization of a chip. To manufacture the known chip module, the individual substrates of the chip carriers are arranged on a continuous substrate carrier, which is connected with the individual substrates via the connection leads extending continuously over the substrate carrier. In the known method, the film-like substrate carrier is used only to connect the connection leads with the substrate.

Known from DE 196 01 203 A1 are a data carrier card and a method of its manufacture, in which the data carrier card consists of a flat, injectionmolded plastic card body with at least one recess, on which three dimensionally guided printed conductors are applied. A chip can

be electrically connected with the printed conductors in the recess, and then have a protective layer cast around it to form the data carrier card.

EP 0 421 343 A2 describes a chip carrier for the connection and electromagnetic shielding of a single chip. The chip carrier has a complex, curved structure with discontinuous connection leads formed on the surface of the chip carrier.

EP 0 682 321 A2 shows a chip carrier to be arranged in a card body. The chip carrier exhibits a carrier substrate with connection leads discontinuously formed on the surface.

EP 0 391 790 A1 describes a chip module or a method of manufacturing an encapsulated chip module with a chip, in which a structured metal film is applied to a carrier film to form connection leads.

FR 2 756 955 A1 describes a method of contacting a chip with a coil on a card-shaped carrier material, which is provided with a printed board arrangement in the form of a coil.

SUMMARY AND OBJECTS OF THE INVENTION

Proceeding from known prior art, the object of the invention is to provide a chip carrier for a chip module or a method of manufacturing a chip module, which exhibits a particularly simple design relative to the known chip modules, and hence opens the door to particularly cost-effective manufacture.

This object is achieved using a chip carrier with ~~the features set forth in claim 1.~~

for forming a chip module with a substrate and connection leads arranged on the substrate. The connection leads are designed like stripes and extend parallel over the substrate. In the chip carrier according to the invention, the connection leads consist of electrically conductive connection strands placed on the substrate, and the substrate is formed by a carrier film. ~~i~~

Designing the connection leads as connection strands that are completely independent of the carrier film makes it possible not to have to manufacture the connection leads based on an expensive etching technique. Therefore, the chip carrier according to the invention consists ~~t~~ of a combination of a carrier film and connection strands, which each represent independent elements in the initial state, so that no special technologies, e.g., the use of an etching process, are required for manufacturing the chip carrier, but rather a simple connecting or joining process, wherein the substrate is directly formed by the carrier film. Having the substrate serve as the carrier film also enables substrates with a particularly flat design.

In a particularly preferred embodiment of the chip carrier, the side of the carrier film opposite the connection strands is provided with at least one additional conductive strand, in which the insulating carrier film is arranged between the connection strands on the one hand and the additional conductive strand on the other, forming an intermediate layer.

Adding this at least one conductive strand on the opposite side of the carrier film yields a capacitor structure that is arranged in a parallel circuit with the chip after the connection

strands have been contacted with a chip. Precisely in the area of transponder technology, this special configuration of the chip module gives rise to the special advantage when contacting the connection strands with a coil unit that the range of the transponder unit formed by combining the chip and coil unit can be distinctly increased.

In particular with respect to the automated manufacture of chip modules using the chip carriers, it proves advantageous to provide the connection strands at least sectionally with a connecting material coating for contacting with the contact metallizations of the chip, so that the chip can be contacted directly on the connecting strands after providing the substrate without any additional intermediate step. This connecting material coating can consist of a connecting solder coating, or a coating of electrically conductive adhesive or the like.

Providing the connection strands at least sectionally with a contact metallization for contacting with the elevated contact metallizations of the chip makes it possible to obtain especially high-quality, i.e., reliable, connections, in particular due to the surface quality of the connection strands as unproved by the contact metallization. Otherwise, of course, connecting strands made out of copper or a copper alloy can be used to produce a direct connection with the contact metallizations of the chip, in particular if the contact metallizations of the chip exhibit a lead/tin alloy or similar alloys with a correspondingly low melting point.

If the connection strands of the chip carrier arc connected with the terminals of the coil

unit, the chip carrier can serve as the basic unit for manufacturing a transponder, wherein the basic unit need only be enhanced by contact with a chip.

Based on the chip module described above, it is also possible, as already mentioned above, to provide a transponder module in which the connection strands contacted with the contact metallizations of the chip are connected according to the invention with terminals of a coil unit.

In the chip module according to the invention, the contact metallizations of the chip are contacted with the top side of the connection strands of the chip carrier. In addition to the fact that the chip module can be manufactured with a simple flip-chip contact, this chip module structure offers the advantage of making the side of the substrate lying opposite the connection strands available for further applications.

If the connection strands contacted with the contact metallizations of the chip are additionally connected with the terminals of a coil unit, a transponder module with an especially simple structure is obtained.

The method according to the invention ~~for~~of manufacturing a chip module involves the following steps:

- applying at least two electrically conductive connection strands to one side of ~~a~~the carrier film, so that the connection strands ~~extend~~lie parallel to each other in a single plane, and extend in a planar direction over the carrier film, and

- contacting contact metallizations of the chip with the connection strands, so that a contact metallization of the chip is contacted with a respective connection strand.

As already emphasized at the outset while describing the structure of the chip module according to the invention, the manufacturing process is characterized by the lowest possible number of steps, due to the fact that the substrate provided with connection leads is realized via a simple combination of connection strands with a carrier film, and the type of contacting according to the invention enables a simple flip-chip contacting.

If the connection strands are contacted with the coil unit before being contacted with the chip, a first portion of the manufacturing process, which can also be executed independently of the subsequent contacting with the chip, yields an intermediate product in the form of a chip carrier, which can be directly used for manufacturing transponder units.

One particularly economic variant of the method according to the invention can be implemented if the connection strands are continuously applied to the carrier film~~ct~~, so that the connection strands and the carrier film are provided as continuous strands, and moved

continuously toward each other in a ~~contacting~~contact area with the generation of an adhesion.

If the carrier film is provided with window openings at defined distances before forming the contact area with the connection strands, so that the window openings in the subsequently formed contact area are covered by the connection strands while forming pocket-like contact receptacles, it becomes possible to manufacture a chip module even without the influence of a continuous process, in which the contact metallizations of the chip are contacted with the bottom side of the connection strands, and the chip itself is located on the side of the carrier film opposite the connection strands.

Therefore, this method variant enables the manufacture of an especially i flat or thin chip module.

A chip module with a capacitor structure can be manufactured in another method variant by placing at least one additional electrically conductive counter-strand on the side lying opposite the side intended for applying the connection strands. _This process can take place before or after applying the connection strands on the carrier film.

One particularly easy and hence cost-effective way of implementing the method is made possible by applying the connection strands and/or at ~~to~~ least one counter-strand on the carrier film in a lamination process.

In this connection, it is also advantageous to use a hot-melt coating to form an adhesion between the connection strands and/or the at least one counter-strand and the carrier film.

An embodiment of the chip module and a variant of the method of manufacturing the chip module shall be explained in greater detail below based on the drawings. ~~Shown in: Fig. 1 is~~

The various features of novelty which characterize the invention are pointed out with particularity in the claims annexed to and forming a part of this disclosure. For a better understanding of the invention, its operating advantages and specific objects attained by its uses, reference is made to the accompanying drawings and descriptive matter in which preferred embodiments of the invention are illustrated.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

Fig. 1 is a top view of a chip carrier for manufacturing a chip module~~, top view,~~

Fig. 2 is a view of the chip carrier shown in Fig. ~~1~~1 with a chip in contacted thereupon to form a chip module;

Fig. 3 is a sectional view of a first embodiment of a chip module~~;~~;

Fig. 4 is a sectional view~~; Fig. 4 is~~ of a second embodiment of the chip module~~;~~;

Fig. 5 is a sectional view~~; Fig. 5 is~~ of a third embodiment of a chip module~~, sectional view~~;

Fig. 6 is a sectional view of an electrical equivalent circuit diagram for the substrate of the chip module shown in Fig. 5;

and

Fig. 7 is a diagrammatic view of a device for performing a variant of the method of manufacturing the chip module.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to the drawings in particular, Fig. 1 shows a top view of a section of a chip carrier strand 10 with a carrier film 11 and connection strands 12 and 13 applied to one side of the carrier film 1~~1~~1.

Fig. 2 shows the chip carrier strand 10 depicted in Fig. 1 with numerous spaced chips 14 contacted on the chip carrier strand 10. As evident from Fig. 2, the chips 14 with their contact metallizations, also referred to as "bumps" in technical parlance, are placed in contact~~ed~~ with connection strands 12, 13 in flip-chip technology in such a way that one bump 15 or 16 is allocated to a connection strand 12, 13 in an electrically conductive manner.

As indicated by separating lines 17 in Fig. 2, chip modules 18 are detached from the composite chip module held together by the chip carrier strand 10 via separating cuts through the chip carrier strand 10 after the chips 14 have contacted the chip carrier strand 10.

Fig. 3 shows a sectional view according to intersecting line III-III in Fig. 2. As evident, chip 14 is in contacted in flip-chip technology with its bumps 15, 16 on the connection strands 12, 13 of the chip carrier 19 separated out of the chip carrier strand 10 along separating lines 17. In this case, the carrier film 11 forming the substrate of the chip carrier 19 consists of kapton, whose top side is covered with the connection strands 12, 13 made out of so-called E copper. To improve the surface quality of the connection strands 12. 13, the latter are coated with a contact metallization in this case. Other electrically non-conductive materials can also be used for the chip carrier 19 or chip carrier strand 10, e.g., epoxy glass, polyester, polycarbonate and polyimide, wherein a flexible design of the carrier film 11, e.g., using polyimide, is advantageous, in particular when using a manufacturing process of the kind explained in greater detail below with reference to Fig. 7.

Fig. 4 shows a variant of a chip module 20 in which the chip 14 is placed in contacted with a bottom side 22 of the connection strands 12, 13, as opposed to the chip module 18 shown in Fig. 3, where the chip 14 is in contacted with a top side 21 of the connection strands 12, 13.

to To this end, pocket-like contact receptacles 23, 24 are formed in the areas of the carrier film 11 of a chip carrier 28 covered by the connection strands 12, 13, and used to accommodate the bumps 15, 16 of the chip 14. Given the appropriate preparation of the surfaces of connection strands 12, 13, e.g., via contact metallization, the bumps 15, 16 can be directly isn contacted with the connection strands 12, 13, or a contacting process as shown in Fig. 4 can be performed, in which a separate bonding material, e.g., soldering material 25 situated

between the bottom sides 22 of the connection strands 12, 13 and the bumps 15, 16 of the chip 14 is additionally provided.

Fig. 5 shows another embodiment of a chip module 26, in which, as opposed to the chip module 18 shown in Fig. 3, a counter-strand 27 is provided on the side of the carrier film ~~11~~ 11 opposite the connection strands 12, 13, which is applied to the carrier film ~~11~~ 11 in the same manner as the connection strands 12,13, and can consist of the same material as the connection strands 12, 13.

The structure shown in Fig. 5 of opposing connection strands 12, 13 separated from each other by an insulating intermediate layer in the form of the carrier layer ~~11~~ 11 on the one hand and the counter strand 27 on the other yields a~~m~~n electric capacitor arrangement whose circuit diagram is shown in ~~f~~Fig. 6. According to Fig. 6, the structure of the substrate 28 yields an electrical serial connection of two capacitors arranged parallel to the chip 14.

Fig. 7 shows a possible variant for manufacturing a chip module, wherein the system design shown in Fig. 7 enables in particular the manufacture of the chip module 20 shown in Fig. 4 in a continuous and interconnected arrangement. To this end, the system diagrammatically shown in Fig. 7 encompasses a supply roll 30 with carrier film 11 wound onto it, which is unrolled in the direction of arrow 31, and wound up at the end of the system on a product roll 32. Located in the area between the supply roll 30 and product roll 32 are two supply rolls 33 and 34 with wound up connection strand 12 or 13. Located between the supply

rolls 33 and 34 on the one hand and the product roll 32 on the other is a laminating roller 35. To manufacture a continuous, band-shaped and interconnected arrangement of chip carriers 28 or chip modules 20, as shown in ~~f~~Fig. 4,

the carrier film 11 is clocked and advanced in the direction of the arrow 31 according to Fig. 7, wherein window openings are incorporated into the carrier film ~~H~~11 at the prescribed clock rate at defined intervals via a stamping device 36 to form the contact receptacles 23, 24 shown in Fig.

4. Downstream of the stamping device 36, the connection strands 12, 13

are supplied to the carrier film 11 from the supply rolls 33, 34, and then connected with the carrier film 1~~+~~1 in a roll slit formed by the laminating roll 35 and a counter-roll 37 in a contact area 38. As a result of this joining or connecting process, the chip carrier 28 shown in cross section in Fig. 4 is therefore generated in continuous form downstream of the laminating roll 35, and wound on the product roll 32. The product roll 32 can now be used as a supply roll for a subsequent manufacturing process for the continuous or clocked contacting of chips 14 with the connection strands 12, 13, thus making it possible to manufacture continuously interconnected chip modules 20 as shown in Fig. 4.

To prepare for a subsequent manufacture of transponder units, coil units can also be contacted with the connection strands after the laminating process. The coils can here be designed as desired. The coils can be arranged on a separate carrier, or have no carrier in a particularly advantageous variant, being applied directly to the carrier film and contacted with

the connection strands. In this connection, the use of wire coils proves advantageous.

While specific embodiments of the invention have been shown and described in detail to illustrate the application of the principles of the invention, it will be understood that the invention may be embodied otherwise without departing from such principles.

ABSTRACT OF THE DISCLOSURE

A chip carrier for ~~forming~~manufacturing a chip module (18), with a substrate and connection leads arranged on the substrate~~, wherein the~~ has connection leads ~~are~~ designed like stripes and ~~extend~~extending parallel over the substrate~~, characterized in that t~~. The connection leads ~~consist of~~are electrically conductive connection strands (12, 13) ~~applied to~~placed on the substrate~~, and t~~. The substrate is formed by a carrier film (11).

~~ABSTRACT The invention relates to a chip carrier for manufacturing a chip module (18), with a substrate and connection leads arranged on the substrate, wherein the connection leads are designed like stripes and extend parallel over the substrate, and wherein the connection leads consist of electrically conductive connection strands (12, 13) placed on the substrate, and the substrate is formed by a carrier film (11).~~

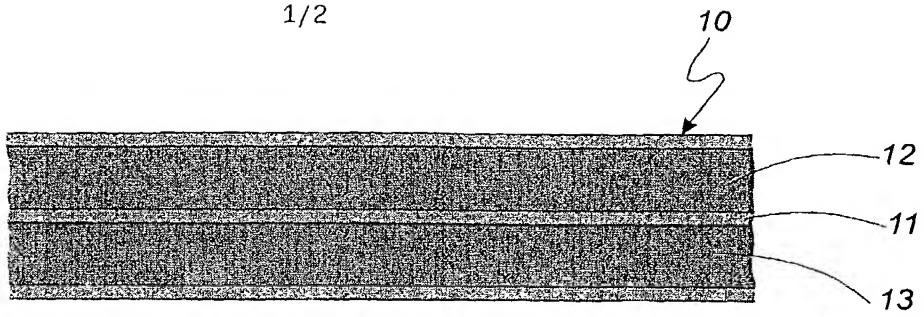

Fig. 1

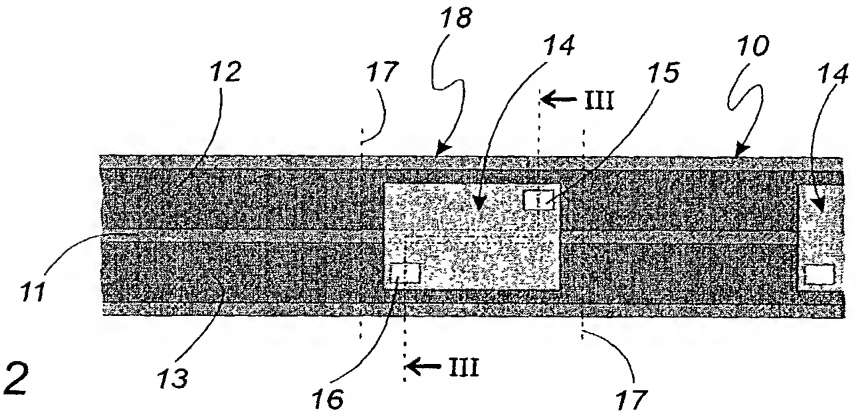

Fig. 2

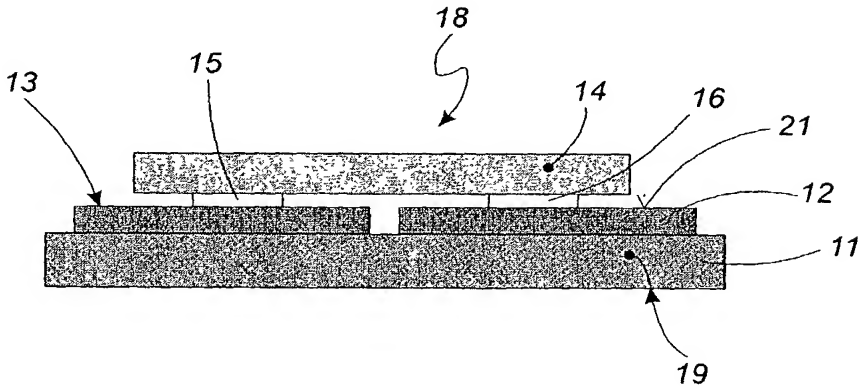

Fig. 3

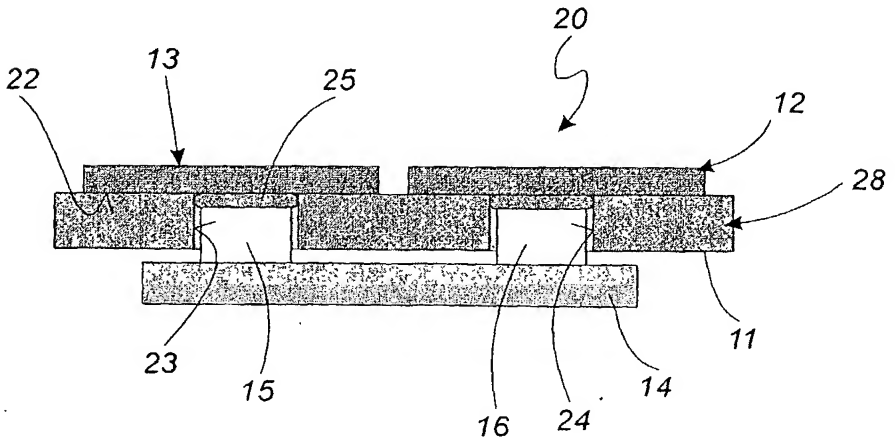

Fig. 4

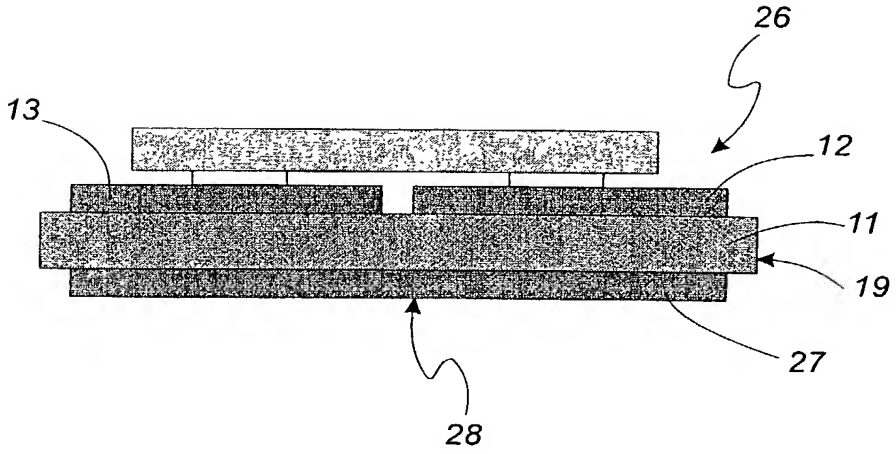

Fig. 5

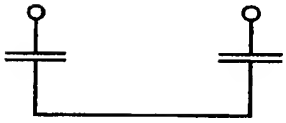

Fig. 6

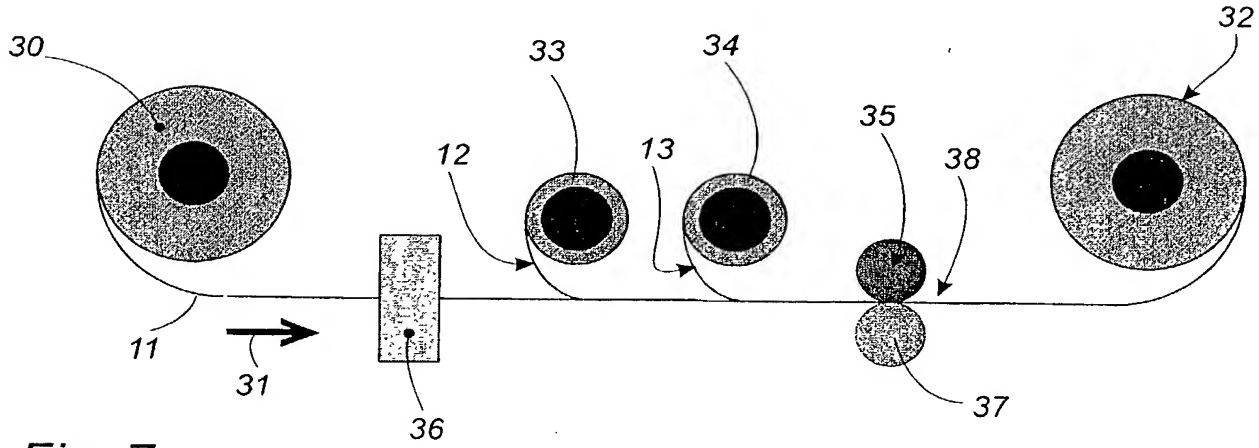

Fig. 7

DECLARATION FOR PATENT APPLICATION

Docket No.70357

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: *CHIP CARRIER FOR A CHIP MODULE AND METHOD OF MANUFACTURING THE CHIP MODULE*

the specification of which

(Check one) [ ] is attached hereto.
[X] was filed as PCT international application
Number PCT/DE00/01396
on 4/May/2000
and was amended under PCT Article 19
on _____

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, 119 (a)-(d) or 365 (b) of any foreign application(s) for patent or inventor's certificate or 365 (a) of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate having a filing date or any PCT international application(s) designating at least one country other than the United States of America by me on the same subject matter having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed
199 20 593.0	Germany	5/May/1999	Yes
(Number)	(Country)	(Day/Month/Year filed)	
(Number)	(Country)	(Day/Month/Year filed)	

[redacted]

(Number) (Country) (Day/Month/Year filed)

I hereby claim the benefit under Title 35, United States Code, 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code 112. I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No) (Filing Date) (Patented, Pending, Abandoned)

(Application Serial No) (Filing Date) (Patented, Pending, Abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: **John J. McGlew, Reg. 17,722; and/or John James McGlew, Reg. 31,903; and/or Hilda S. McGlew Reg. 30,295; and/or Theobald Dengler, Reg. 34,575; and/or Keith D. Moore, Reg. 44,951.**

Address all calls to: John James McGlew at telephone no. (914) 941-5600
Address all correspondence to:

McGLEW AND TUTTLE, P.C.
SCARBOROUGH STATION
SCARBOROUGH, NEW YORK 10510-0827

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

[redacted]

Full name of sole or first inventor David FINN

→Inventor's signature _____ →Date 11.6.02
Residence Edelsbergstr. 2 D-87629 Füssen-Weissensee, GERMANY
CitizenshipIreland
Post Office Address Edelsbergstr. 2, D-87629 Füssen-Weissensee, GERMANY

Full name of second inventor Manfred RIETZLER

→Inventor's signature _____ →Date 2.5.02
ResidenceAm Alsterberg 10, D-87616 Marktoberdorf, GERMANY CitizenshipGermany
Post Office Address Am Alsterberg 10, D-87616 Marktoberdorf, GERMANY

Full name of third inventor _____

→Inventor's signature _____ →Date _____
Residence _____ Citizenship _____
Post Office Address _____

Full name of fourth inventor _____

→Inventor's signature _____ →Date _____
Residence _____ Citizenship _____
Post Office Address _____

Full name of fifth inventor _____

→Inventor's signature _____ →Date _____
Residence _____ Citizenship _____
Post Office Address _____

Full name of sixth inventor _____

→Inventor's signature _____ →Date _____
Residence _____ Citizenship _____
Post Office Address _____

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